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A REPLENISHMENT MODEL FOR VMI WAREHOUSE OF LED-CM PLANTS

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ABSTRACT

Purpose- The LED Chip Manufacturing (LED-CM) is an important process in the LED supply chain. Due to customer pressure or to providing better services in order to enhance competitiveness, the Vendor Managed Inventory (VMI) strategy is applied in LED-CM plant in recent years. The chips in the VMI warehouse of the customers must meet the specifications of the customer requirements. Basically, Chips of a specification of the customer requirements compose of the chips of different bins. A bin is defined by the definite electrical functions of LED chips. Deciding how many chips of each feasible bin must be allocated to a replenishment order (RO) affects the performance of VMI in LED-CM plant.

Methodology- A model of allocating chips from bins to ROs for LED-CM plants is proposed in this paper. Three objectives, i.e., maximizing ROs of delivery, maximizing throughput of delivery and maximizing the total left chips of the feasible bins of potential ROs, are considered in the proposed model to obtain the best result.

Findings- The obtained ROs of delivery or throughput of delivery could serve as a valuable informance for LED-CM plants.

Conclusion- Results show that employing the proposed methodology can facilitate LED-CM plants to implement the VMI service effectively.

Keywords: LED chip manufacturing, vendor managed inventory, peplenishment order, chips allocation, optimal inventory allocation models JEL Codes: C39, C61

1. INTRODUCTION

The Light-Emitting Diode (LED) is a popular green industry these years. The major processes of the LED supply chain are material substrate process, upstream process, midstream process and downstream process etc (Wu et al., 2013). The LED chip manufacturing (LED-CM) plant is in the midstream of the LED supply chain. Its manufacturing process is not only complex but also unstable. Furthermore, the quality of the LED chips will determine the function of the subsequent applications (Chang et al., 2012, Scholand and Dillon, 2012). Therefore, the LED-CM plants are important in the LED supply chain.

Basically, the input material of LED-CM plants is EPI (epitaxial material) and the final products are LED chips. An EPI can be cut or broken into several or several ten thousands LED chips depending on its size. The electrical functions of all chips in an EPI will be gradient distribution due to the special feature in the frontend process. In other words, the electrical function of each chip in an EPI is different. Those chips with non-identical electrical functions must be sorted into different bins in the sorting station of the backend process.

The required electrical specification of an order of LED chips will be transferred to its feasible bins by the production planner. Generally, the specification of an order can be fulfilled by the chips of several feasible bins. Therefore, the feasible bins of different specification of orders are required variably. The make-to-order (MTO) production strategy (Croxton 2003, Ebadian *et al.*, 2011, Gao *et al.*, 2008) is thus a general production strategy for the LED-CM plants to satisfy the various requirements of customers. However, the desired chips or bins in an EPI are unstable output for a manufacturing order (MO). Because the different bin distributions in an EPI will be determined by the different EPI or process parameters in the frontend process. The more by-products (chips of undesired bins) will be accompanied by a MO due to the feature of gradient distribution of bins in an EPI. Therefore, the inventories of by-products are accumulated more and more in the warehouse of LED-CM plants.

Due to customer pressure or to providing better services in order to enhance competitiveness, the Vendor Managed Inventory (VMI) strategy is forced to be applied in LED-CM plant in recent years. VMI also known as continuous replenishment, supplier-managed inventory, or consignment inventory, it is a supply chain strategy where the vendor is given the responsibility of managing the customer's stock (Angulo *et al.*, 2004). Under the VMI, the customers provide the vendor with access to their real-time inventory level (Mateen et al., 2015, Ryu *et al.*, 2013). The vendor decides and manages when and how much to deliver (Razmi *et al.*, 2010). The task of vendor is to provide flowed products on the supply chain. When the inventory level is below a predetermined level, the vendors will sent out orders to replenish stocks (Lan *et al.*, 2011). In other words, the customer provides the vendor with inventory information and the vendor uses this information to monitoring inventory or placing orders.

VMI was first implemented by Wal-Mart and has become more popular in the last 20 years (Ryu *et al.*, 2013). It has been widely used by various companies in diverse industries including Shell Chemicals, HP (Cetinkaya & Lee 2000, Mishra and Raghunathan 2004), Elec-trolux (De *et al.*, 2005), Nestle and Tesco, Boeing, Intel, etc (Chakraborty *et al.*, 2015, Ryu *et al.*, 2013). The VMI leads the supplier to increase replenishment frequencies with smaller quantities and reduces inventory level for all involved in distribution and the supply chain (Chen and Chang, 2010, Dong *et al.*, 2007, Rad *et al.*, 2014). It also causes greater inventory cost saving and improved customer service levels (Achabal *et al.*, 2000, Kang and Kim 2012, Rad *et al.*, 2014, Williams 2000, Zavanella and Zanoni, 2009). VMI is the wave of the future and the concept will revolutionize the distribution channel. It offers a competitive advantage for customers with respect to higher product availability and provides the supplier with opportunities to improve production and replenishment efficiencies (Rad *et al.*, 2014, Ryu *et al.*, 2013). Summarily, VMI not only has the ability to reduce costs, but also to improve service levels and create business opportunities for both parties in the supply chain. Through VMI, production and inventory control efficiency can be significantly improved (Razmi *et al.*, 2010).

This paper aims at the issues of replenishment and inventory between LED-CM plant and the VMI warehouse. Implementing VMI in LED-CM plant is complex because the special features of specification of a product composed of the chips of different bins exist in this plant. Although the allocations of inventory to orders is a popular research topics (Fowler *et al.*, 2010, Hop and Kawtummachai 2005, Hoque 2008, Monthatipkul and Kawtummachai, 2007, Ozbayrak *et al.*, 2006, Pibernik and Yadav,, 2009, Razmi and Rafiei 2010, Shafieezadeh and Sadegheih, 2014), the allocation of chips from bins to replenishment orders (Ros) for LED-CM plants is sparse in the literatures. Deciding how many chips of each feasible bin must be allocated to a replenishment order (RO) affects VMI performance in LED-CM plants; a model of allocating chips from bins to ROs for LED-CM plants is thus proposed in this study. The proposed methodology will facilitate LED-CM plants to implement the VMI service effectively. This paper is divided into eight sections including introduction, background of LED-CM plants, methods, problems of implementing VMI in LED-CM plants, a replenishment model, numerical example and application, discussions and conclusion.

2. BACKGROUND OF LED-CM PLANTS

2.1. The Product Specifications

The specifications of the LED chip are several, such as structure, size, electrical functions, voltage or customized requirements etc., the major specification is the electrical functions, i.e., lightness and wavelength. Therefore, these two functions are utilized as the product specifications of the RO in the following discuss. For example, for the yellow light, the wavelength is between 584nm and 594nm and lightness is between 0mcd and 250mcd.

2.2. Bin Definition

In order to sort the different specification of LED chips, bin concept is utilized in the LED-CM plants. A bin is defined by the definite electrical functions of LED chips, i.e., a definite lightness grade and waveband. The lightness of a color light is divided into several lightness grades (i.e., *L* grades) depending on the requirements of users. For example, the lightness of the yellow light is between 0mcd and 250 mcd and is divided into 5 grades as shown in Table 1. Similarly, the wavelength is also divided into several wavebands (i.e., *W* wavebands). For example, the yellow wavelength is between 584nm~594nm and is divided into 5 wavebands as shown in Table 1. Therefore, *L* x *W* bins are utilized to sort the LED chips with different lightness and waveband in the backend process. For example, in Table 1, 25 (=5 x 5) bins are utilized to sort the LED chips and the LED chips with the lightness between 50mcd and 100mcd and wavelength between 586nm and 588nm will be

sorted into the (2, 2) or 7^{th} bin. However, the number of lightness grade and waveband is not definite but can be decided by a LED-CM plant. For example, as shown in Table 2, there are only 9 (=3x3) bins. It is a simplified example of Table 1 and will be utilized in the following discussion.

| | Bin # | | | | Waveband (nm) | (w) | |
|------------|----------------|-------|---------|---------|---------------|---------|---------|
| | (<i>I.w</i>) | | 584~586 | 586~588 | 588~590 | 590~592 | 592~594 |
| | () / | | 1 | 2 | 3 | 4 | 5 (W) |
| | 0~50 | 1 | (1,1) | (1,2) | (1,3) | (1,4) | (1,5) |
| Lightness/ | 50~100 | 2 | (2,1) | (2,2) | (2,3) | (2,4) | (2,5) |
| Grade | 100~150 | 3 | (3,1) | (3,2) | (3,3) | (3,4) | (3,5) |
| (mcd)/(/) | 150~200 | 4 | (4,1) | (4,2) | (4,3) | (4,4) | (4,5) |
| | 200~250 | 5 (L) | (5,1) | (5,2) | (5,3) | (5,4) | (5,5) |

Table 1: An Example of Bin Definition for Yellow LED Chips

Table 2: The Bin Definition and Chips (Inventory) in Each Bin

| Ching | in a hin | | v | Vaveband (nm) (v | v) | |
|------------|---------------|---|---------|------------------|---------|-------|
| (yk ch | $\frac{1}{h}$ | | 584~587 | 587~590 | 590~594 | Total |
| (^K CI | | | 1 | 2 | 3 | |
| Lightness/ | 0~100 | 1 | 455 | 900 | 657 | 2012 |
| Grade | 100~200 | 2 | 757 | 847 | 757 | 2361 |
| (mcd)/(/) | 200~300 | 3 | 551 | 565 | 400 | 1516 |
| Т | otal | | 1763 | 2312 | 1814 | 5889 |

2.3.Chips in a Bin

The chips in a bin are all with the specification of this bin after the sorting operation of the backend process. Therefore, these chips are the inventory of this bin and can be utilized to fulfill the consecutive ROs. As shown in Table 2, the chips in the 1^{st} bin are 455k and in the 5^{th} bin are 847k etc.

2.4. Replenishment Order (RO)

The RO is defined as a replenishment order of the VMI warehouse. The task of LED-CM plant is to provide flowed products on the supply chain. When the inventory level is below a predetermined level, the LED-CM plant will put forward a RO to replenish stocks actively. Both quantity and product specifications are the basic requirements of a RO.

2.5. Feasible bins of a RO

A feasible bin of a RO is defined to be that its lightness grade and waveband are within the specifications of this RO. When a LED-CM plant put forward a RO, the planner must first transfer the required lightness and wavelength specification of this RO to the feasible internal lightness grade and waveband specification of this plant. The feasible internal lightness grade and waveband specification of this plant. The feasible internal lightness grade and waveband specifications must be within the required lightness and wavelength specification require that those internal specifications must be within the required lightness and wavelength specification are defined to be the feasible bins of the RO. Then, the bins whose specifications are within the feasible internal specification of the 1st RO are 0~210mcd and 584~589mm respectively. Based on the bin definition in the Table 2, the planner will transfer the required lightness and wavelength specification of the 1st RO are 0~210mcd and 584~589mm respectively. Based on the bin definition in the Table 2, the planner will transfer the required lightness grade and 1~2 waveband. Then the bins whose specifications are within the feasible internal specification are 1st, 2nd, 4th and 5th bin respectively. Therefore, as shown the shadow grid in Table 2, the feasible bins of the 1st RO are 1st, 2nd, 4th and 5th bin. That is the chips in these four bins can meet the required specification of 1st RO. The feasible bins of a RO are supposed to be known in this paper because they can be defined easily in the practical applications.

| RO | Demined Otra (ada | Customer Re | equired Spec. | Fe | easible int | ternal Sp | ec. | | Faasih | | |
|-----|--------------------------|-------------|---------------|-----------------|-----------------|-----------------|-----------------|---|--------------|-----------------------------|---|
| # | Chips) (r _i) | Lightness | Wavelength | Lightne | ss Grade | Wave | eband | | Feasib (F | ie Bins B _i) | |
| (i) | | (mcd) | (nm) | ll _i | lu _i | wl _i | wu _i | | | | |
| 1 | 370 | 0~210 | 584~589 | 1 | 2 | 1 | 2 | 1 | 2 | 4 | 5 |
| 2 | 440 | 0~110 | 584~595 | 1 | 1 | 1 | 3 | 1 | 2 | 3 | - |
| 3 | 180 | 0~310 | 583~588 | 1 | 3 | 1 | 1 | 1 | 4 | 7 | - |
| 4 | 310 | 0~300 | 589~594 | 1 | 3 | 3 | 3 | 3 | 6 | 9 | - |
| 5 | 430 | 0~210 | 586~595 | 1 | 2 | 2 | 3 | 2 | 3 | 5 | 6 |
| 6 | 350 | 0~300 | 586~591 | 1 | 3 | 2 | 2 | 2 | 5 | 8 | - |
| 7 | 950 | 180~300 | 584~594 | 3 | 3 | 1 | 3 | 7 | 8 | 9 | - |
| 8 | 1320 | 90~310 | 586~594 | 2 | 3 | 2 | 3 | 5 | 6 | 8 | 9 |
| 9 | 370 | 90~220 | 583~594 | 2 | 2 | 1 | 3 | 4 | 5 | 6 | - |
| 10 | 1000 | 90~300 | 584~590 | 2 | 3 | 1 | 2 | 4 | 5 | 7 | 8 |

| Table 3: Example: | of the Require | ments of Ten RO | s and Feasible Bins |
|-------------------|----------------|-----------------|---------------------|
|-------------------|----------------|-----------------|---------------------|

2.6. Upgrade of Specification Issue

If the chips which fulfill a RO are too focus in some bins of the feasible bins of this RO, an upgrade of specification issue is occurred. For example, as shown in Table 5, the required quantity of the 2^{nd} RO is 440k and its feasible bins are 1^{st} , 2^{nd} and 3^{rd} bin respectively. Although the chips of any bin of these three bins are greater than 440k, the 2^{nd} RO can't be fulfilled only by the chips of one or two bins of these three bins. Otherwise, an upgrade specification of the 2^{nd} RO occurs. Two drawbacks of upgrade specification will be found. The first is that the customer will complain too bright for this lot if this customer requires more uniform bright in his application. The second is that this customer will require the narrow specification of the next ROs in the same price. However, the more narrow specification it is, the more difficult to be fulfilled it is. In order to avoid the upgrade issue, generally, a required minimum ratio quantity of a feasible bin of a RO will be defined in the LED-CM plants, i.e., 5% etc.

3. METHODS

3.1. Implementation of VMI in LED-CM Plants

When the inventory level of VMI warehouse is below a predetermined level, the LED-CM plant will integrate the requirements of VMI customers and put forward the ROs. The inventories of LED-CM plant are utilized first. If the inventory of LED-CM plant is not enough to meet the requirements of VMI customers then LED-CM plant puts forward the MOs to replenish actively. Structure Diagram of VMI service in LED-CM plant is shown as Fig 1. The RO implement process diagram of the VMI in LED-CM plant is shown as Figure 2. For VMI objective, it is utilized the least inventory to fulfill all the ROs. If inventory of those bins are allocated well, the LED-CM plant will not retain much of the inventory. Otherwise, in addition to the original inventory, the LED-CM plant is necessary to reserve more inventory to fulfill the left ROs, increases the inventory cost and more risk.

3.2. Notations and Descriptions

I: The total number of ROs to be fulfilled.

- *i*: An index denoting the identification of ROs, *i* =1,2..*I*.
- *FB_i*: The set of the feasible bins of the i^{th} RO, i = 1, 2... I.



Figure 1: Structure of VMI Service in LED-CM Plant

RO -Replenishment Order MO-Manufacturing Order





M: The maximu

m: An index denoting the identification of bins, *m*=1,2..*M*..

L: The maximum range of lightness grade.

I: An index denoting the grade of lightness, *I*=1,2..*L*.

 I_{i} : The lower bound lightness grade of the required specification of the i^{th} RO, i = 1, 2...

 lu_i : The upper bound lightness grade of the required specification of the i^{th} RO ,i = 1, 2... l.

W: The maximum range of wave band.

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- w : An index denoting the waveband of wavelength, w=1,2..W.
- wl_i : The lower bound wave band of the required specification of the i^{th} RO, i = 1, 2... I.
- *wu*_{*i*}: The upper bound wave band of the required specification of the i^{th} RO, i = 1, 2... I.
- b_m : The initial chips (inventory) in the m^{th} bin , m=1,2..M.
- $\dot{b_m}$: The final left chips (inventory) in the m^{th} bin , m=1,2..M.
- d_{im} : The number of chips in the m^{th} bin allocated to RO $_i$, i=1,2..I, m=1, 2, ..., M.
- r_i : The required quantity of the i^{th} RO, i=1,2...
- β_i : The required minimum ratio of quantity of a feasible bin for the i^{th} RO to avoid the upgrade of specification issue, $0 < \beta_i < 0.1, i = 1, 2...$
- v_i : The total chips in the feasible bins of the i^{th} RO, i = 1, 2...I
- k: Abbreviation of kilo, i.e., 1000.

3.3. The Allocation and Assumptions of LED-CM Plants

The assumptions of allocating chips from feasible bins to ROs can be described as follows.

- (1) The specifications of LED chips of a LED-CM plant compose lightness and wavelength. The lightness is divided into *L* grades and wavelength is divided into *W* wavebands.
- (2) There is *M* (=*L* x *W*) bins totally. The indexed number (*m*) of each bin is defined by the lightness grade (*l*) and waveband (*w*) as shown in Equation (1).

$$m = L^*(l-1) + w, \quad l = 1, 2, . L, \quad w = 1, 2, . W$$
 (1)

- (3) Each bin (*m*) has an initial chips (inventory), i.e., b_m , m=1,2,...M.
- (4) There are *I* ROs to be fulfilled by the initial chips in the *M* bins. The required quantity of the RO_{*i*} (*i*=1,2...*I*) is r_i chips. And the feasible bins for the required specification of RO_{*i*} are as shown in Equation (2).

$$FB_{i} = \{(l,w), I|_{i} \leq l \leq lu_{i}, w|_{i} \leq w \leq wu_{i}\} = \{m, m = L^{*}(l-1) + w, I|_{i} \leq l \leq lu_{i}, w|_{i} \leq w \leq wu_{i}\}, i=1,2, ...l$$

That is the chips allocated to the i^{th} RO must be from its feasible bins.

- (5) A minimum ratio of quantity for a feasible bin of the i^{th} RO is required to avoid the upgrade of specification issue. This ratio is a joint decision by the LED-CM plants and between 0% and 10% generally, i.e., $0<\theta_i<0.1$.
- (6) No partial fulfillment is allowed. That is the total initial chips allocated to the *i*th RO cannot be less than its required quantity. Otherwise it is dummy RO.

3.4. The Matrix for Allocation of Chips From Bins to ROs

The allocation of chips from bins to ROs can be modeled as a matrix for the allocation of chips from bins to ROs (MACBRO). The four steps are described as below.

Step 1: Collect the basic data of a MACBRO. There are an index denoting the identification of ROs, required quantity of each RO in the left two columns, an index denoting the identification of bin in the first row, the initial chips (inventory) of each bin in the second row and the grids of feasible bins of each RO shown in shadow in the middle parts as shown in Table 4.

Step 2:

A. Select the allocation method to allocate the chips of each RO. (for example, average allocation method) The allocated chips to each RO must be from its feasible bins as shown in the Equation (3). Furthermore, it formulates that the total allocated chips to each RO must equal to its required quantity. If there are redundancies, then allocate 1k to any feasible bin randomly until finish it.

$$\sum_{m \in FB_{i}} d_{im} = r_{i}, \quad i = 1, 2..I$$
(3)

For example, the bins of 1^{st} , 2^{nd} , 4^{th} and 5^{th} are feasible bins of 1^{st} RO. They are allocated 92k (=370k/4) with average allocation method. There are 2k redundancies allocated 1k to 4^{th} and 5^{th} feasible bin. It is shown as Table 5.

B. In order to avoid the upgrade of specification issue. The ratio is between 0% and 10% generally, i.e., $0 < \beta_i < 0.1$ as shown in Equation (4).

$$d_{im} \ge \beta_i \times r_i \quad , \quad i = 1, 2. I, \quad m \in FB_i \tag{4}$$

Step 3: Check if the total initial chips (inventory) in the feasible bins of the *i*th RO is greater than or equal to the required quantity of this RO as shown in Equation (5). If yes, then go to next step. If not, then fills up zero in all spaces of feasible bin of this RO, and skip next RO and go to step 2.

$$v_i = \sum_{m \in FB_i} b_m \ge r_i \text{ , } i=1,2, \dots$$
(5)

For example, the 7th, 8th and 9th bin is the feasible bin of 7th RO. The initial inventory of 7th bin is 491k (=551k-60k). The initial inventory of 8th bin is 448k (=565k-117k). The initial inventory of 9th bin is 296k (=400k-104k). The total initial inventories in the feasible bins of 7th RO is 1235k (=491k+448k+296k), which is greater than its total required quantity (i.e., 950k). However, the total initial inventories in the feasible bins of 8th RO is 1196k, which is less than its total required quantity (i.e., 1320k) as shown in Table 5, then fills up zero in all spaces of feasible bin of this RO. It skips to 9th RO and starts from step 2.

Step 4: The total allocated quantity in the feasible bin from 1st RO to ith RO must be less than or equal to its initial chips as shown in Equation (6). The final left chips in a bin will not be less than zero

$$\sum_{i=1}^{I} d_{im} \le b_m, \quad m = 1, 2...M$$
(6)

For example, there are 316k, 316k and 317k chips allocated to 7^{th} , 8^{th} and 9^{th} bin of 7^{th} RO respectively. The initial inventory of 7^{th} bin (491k) is great than 316k. The initial inventory of 8^{th} bin (448k) is great than 316k. Due to the initial inventory of 9^{th} bin (296k) is less than 317k, the 9^{th} bin of 7^{th} RO must be allocated 296k. The left required quantity of 7^{th} RO is 654k (=950k-296k). It is allocated 327k to 7^{th} and 8^{th} bin of 7^{th} RO. It is shown in Table 5.

| Bi | n # (<i>m</i>) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | TT |
|------------------|--------------------------------|-----|-----|-----|-----|------------|------------|-----|-----|-----|------|
| Init | . Inv.(<i>b_m</i>) | 455 | 900 | 657 | 757 | 847 | 757 | 551 | 565 | 400 | 5889 |
| RO# (<i>i</i>) | Qty(r _i) | | | | A | llocated Q | uantity (d |) | | | |
| 1 | 370 | | | | | | | | | | |
| 2 | 440 | | | | | | | | | | |
| 3 | 180 | | | | | | | | | | |
| 4 | 310 | | | | | | | | | | |
| 5 | 430 | | | | | | | | | | |
| 6 | 350 | | | | | | | | | | |
| 7 | 950 | | | | | | | | | | |
| 8 | 1320 | | | | | | | | | | |
| 9 | 370 | | | | | | | | | | |
| 10 | 1000 | | | | | | | | | | |
| Final | Inv. ($b_m^{'}$) | | | | | | | | | | |

Table 4: The MACBRO for Example in Table 3 (Unit: k chips)(before chips allocating process)

| Bi | in # (<i>m</i>) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | TT |
|------------------|--------------------------------|-----|-----|-----|-----|-----------|------------|-----|-----|-----|------|
| Init | . Inv.(<i>b_m</i>) | 455 | 900 | 657 | 757 | 847 | 757 | 551 | 565 | 400 | 5889 |
| RO# (<i>i</i>) | Qty(r _i) | | | | A | located Q | uantity (d | im) | | | |
| 1 | 370 | 92 | 92 | | 93 | 93 | | | | | 370 |
| 2 | 440 | 146 | 147 | 147 | | | | | | | 440 |
| 3 | 180 | 60 | | | 60 | | | 60 | | | 180 |
| 4 | 310 | | | 103 | | | 103 | | | 104 | 310 |
| 5 | 430 | | 107 | 107 | | 108 | 108 | | | | 430 |
| 6 | 350 | | 116 | | | 117 | | | 117 | | 350 |
| 7 | 950 | | | | | | | 327 | 327 | 296 | 950 |
| 8 | 1320 | | | | | 0 | 0 | | 0 | 0 | 0 |
| 9 | 370 | | | | 123 | 123 | 124 | | | | 370 |
| 10 | 1000 | | | | 357 | 358 | | 164 | 121 | | 1000 |
| Final | Inv. (B_m) | 157 | 438 | 300 | 124 | 48 | 422 | 0 | 0 | 0 | 1489 |

Table 5: Results of the MACBRO for the Example in Table 3 (Unit: k chips)

4. PROBLEMS OF IMPLEMENTING VMI IN LED-CM PLANTS

Because only the chips in the feasible bins of the inventory can meet the required specification of the ROs, the shipment of the ROs is then based on the total chips of these feasible bins. If the chips of these feasible bins of the inventory are great than the total required quantity of all ROs, they should be fulfilled. However, some of ROs still cannot be fulfilled, because of a variety of different combinations in allocation issue. If the chips of these feasible bins of the inventory are less than the total required quantity of all ROs, the allocation is much more complex.

Three main issues will affect the result of implementing VMI in LED-CM Plants. The first is how to achieve the maximum ROs. The more ROs are delivered, the less MO is put forward. The second is how to consume the maximum inventory of LED-CM plant. The less inventories remains, the less manufacturing quantity requires. Therefore, the manufacturing overhead reduces and finally the profit increases. The third is how to control the total left chips of the bins of some hot specifications or ROs. If those chips belong to the feasible bins of some popular or hot specifications ROs, the possibility of being utilized in near future will be higher. And hence the competitiveness of LED-CM plants is improved.

For example, as shown in Table 5, the total required quantities of the ten ROs are 5720k chips. There are 5889k chips of the inventory. The total required quantities of the ten ROs are less than the chips of the inventory. Therefore, the ten ROs should be fulfilled by the inventory of their feasible bins immediately. Due to allocation limit, there are only nine ROs can be fulfilled.

In the case of Table 5, suppose that the 8th RO is allocated in front of the 7th RO. The required quantity of the 8th RO is 1320k chips. There are 2563k chips of initial inventory in the feasible bins of the 8th RO and these chips are sufficient for the required quantity of this RO. There are 341k, 341k, 342k and 296k allocated to the 5th, 6th, 8th and 9th bin of 8th RO respectively according to average allocation method. Therefore, the left chips in each feasible bin, i.e., 5th, 6th, 8th and 9th are 188k, 205k, 106k and 0k chips respectively. After allocated to the 8th RO, the total chips in the feasible bins of the 7th RO is failed to be fulfilled by the chips of its feasible bins. However, if the allocating decision of the 8th RO changes to be that the chips of each feasible bins, i.e., 5th, 6th, 8th and 9th etc., allocated to this RO are 520k, 520k, 140k and 140k chips respectively. The left chips in these feasible bins are then 9k, 26k, 308k and 156k chips respectively. The total left chips in the feasible bins of the 7th RO (i.e., 950k chips) in the feasible bins of the 7th RO (i.e., 950k chips). The 7th RO (i.e., 950k chips). The 7th RO (i.e., 950k chips) in the feasible bins are then 9k, 26k, 308k and 156k chips respectively. The total left chips in the feasible bins of the 7th RO (i.e., 950k chips). The 7th RO are then 955k (491k+308k+156k) chips which are greater than the required quantity of the 7th RO (i.e., 950k chips). The 7th RO (i.e., 950k chips). The 7th RO (i.e., 950k chips). The 7th RO can thus be fulfilled by the chips of its feasible bins.

An allocating decision problem will be confronted by the planner and will affect the number of ROs and throughput of delivery. The decision problem is to decide how many chips of each feasible bin must be allocated to a RO. Although this planner can have many choices, his allocating decision will affect the possible fulfillment of other ROs.

In order to achieve more ROs of delivery, higher throughput of delivery or lower left inventory, some objectives of management and constraints are required to effectively complete the decision problem of MACBRO. A model of the allocation of chips from bins to ROs is therefore proposed in the next section.

5. A REPLENISHMENT MODEL

In order to achieve the best performance of the MACBRO, several objectives are considered in this research. They are: (1) maximizing ROs of delivery; (2) maximizing throughput of delivery; and (3) maximizing the total left chips of the bins of some hot specifications or ROs. In dealing with the multiple objective decision-making problem, one of the three objectives is taken as the main objective and the other two are taken as constraints by giving them upper bounds.

5.1. Notations and Descriptions

 e_i : An flag to represent the i^{th} RO to be fulfilled or not, i=1,2...I.

 s_i : The total chips allocated to the i^{th} RO, i = 1, 2... I.

 t_{im} : The planned number of chips in the m^{th} bin allocated to RO_i, *i*=1,2..*I*, *m*=1, 2, .. *M*.

H: The set of hot specifications or ROs.

5.2. Objective Functions

(1) First objective: maximizing ROs of delivery

$$Max \quad z_1 = \sum_{i=1}^{I} e_i \tag{7}$$

The purpose of the first objective is to deliver the ROs as most as possible via the existing chips of LED-CM plants. Because these ROs can be fulfilled by the existing chips, they will be quickly delivered and do not require wait for the long manufacturing lead time. This objective will be important if the required quantities of all ROs are greater than the total initial chips of all bins.

(2) Second objective: maximizing throughput of delivery

$$Max \quad z_2 = \sum_{i=1}^{I} s_i \tag{8}$$

Two benefits will be gained for maximizing the throughput of delivery. The first is the more throughput of delivery is the less inventories remains. The second is the more throughput of delivery is the less manufacturing quantity requires. This objective is more effective if the required quantities of all ROs are greater than the total initial chips of all bins.

(3) Third objective: maximizing the total left chips of the feasible bins of potential specification or ROs.

$$Max \quad z_3 = \sum_{m \in FB_j, j \in H} \dot{b}_m \tag{9}$$

The chips of some bins may be left over from the bin allocating process. For example, 422k chips of the 6th bin are not used and left in Table 5. Those left chips will be utilized to fulfill the popular or hot specifications ROs. Therefore, those left chips of the feasible bins of hot specifications are required as many as possible in the bin allocating process.

5.3. Constraints

Based on the requirements of the decision problem of allocating chips from bins to ROs in LED-CM plants, some constraints must be followed for effectively operating the MACBRO and will be described in this section.

(1) The allocated chips to a RO must come from its feasible bins. It formulates that the total allocated chips to a RO must be equal to its required quantity as shown in Equation (10). It is identical to Equation (3).

$$\sum_{m \in FB_i} d_{im} = r_i, \quad i = 1, 2..I$$
(10)

(2) The planned allocated quantity to a feasible bin of a RO must not be less than the minimum quantity of the required quantity of this RO to avoid the upgrade of specification issue, as shown in Equation (11).

$$t_{im} \ge \beta_i \times r_i \quad , \quad i = 1, 2..I, \quad m \in FB_i \tag{11}$$

(3) Not all ROs can be fulfilled especially when the total initial chips are not enough for all ROs. Therefore, it is required to determine if a RO is fulfilled or not before this RO is allocated chips. As shown in Equation (12), the digit of the flag is number one if the RO is fulfilled. Otherwise, it is zero.

$$e_{i} = \begin{cases} 1, \text{ for the } i^{th} \text{ order fulfilled} \\ 0, \text{ otherwise} \end{cases}, \quad i = 1, 2..I \tag{12}$$

For example, in Table 5, The 1st RO is fulfilled, the digit of the flag is 1. The 8th RO is failed to be fulfilled, then the digit of the flag is 0.

(4) The total allocated chips to a RO must consider if the RO is fulfilled or not, as shown in Equation (13). That is the total allocated quantity from the feasible bins of a RO must be equal to its required quantity if this RO is fulfilled. Otherwise, the total allocated quantity from the feasible bins of this RO must be zero.

$$s_i = e_i \times \sum_{m \in FB_i} d_{im}, \quad i = 1, 2..I$$
(13)

(5) The allocated quantity from a feasible bin of a RO must consider if the RO is fulfilled or not, as shown in Equation (14). That is the allocated quantity from a feasible bin of a RO must be equal to its planned allocated quantity if this RO is fulfilled. Otherwise, the allocated chips from a feasible bin of this RO must be zero.

$$d_{im} = e_i \times t_{im} \quad , \quad i = 1, 2..I, \quad m \in FB_i \tag{14}$$

(6) The total allocated quantity in the feasible bin from 1st RO to ith RO must be less than its initial chips as shown in Equation (15). It is same with Eq.(6). Therefore, the final left chips in a bin will not be less than zero if the initial chips are not be used up as shown in Equation (16).

$$\sum_{i=1}^{I} d_{im} \le b_m, \quad m = 1, 2..M \tag{15}$$

$$\dot{b}_{m} = b_{m} - \sum_{i=1}^{I} d_{im} \ge 0, \quad m = 1, 2...M$$
 (16)

(7) The upper and lower bounds of decision variables are defined as Equation (17).

$$d_{im}$$
, t_{im} and s_i are all non-negative integer, $\forall i, m$ (17)

6. NUMERICAL EXAMPLE AND APPLICATION

To effectively compare these two models, the example shown in Table 3 is utilized to demonstrate its applicability.

6.1. Numerical Example

Assume that the LED-CM plant provides VMI service to three customers, which are X, Y and Z respectively. It is shown as Figure 1. The specifications of the LED chips in this example are sorted to nine bins (i.e., 3x3 bins). The initial chips (inventory) in each bin are shown in Table 2. In order to avoid the upgrade of specification issue, a 1% minimum ratio of quantity is required for a feasible bin of each RO. Integrating the requirements of three VMI customers, the LED-CM plant has ten ROs. The required quantity and specifications of these ROs are shown in Table 3.

When using the average allocation replenishment method, a result of MACBRO for the example in Table 3 is achieved as shown in Table 5. The total chips in all bins which are 5889k are greater than the total required quantity of the ten ROs, i.e., 5720k. Due to allocation limit, it is still not fulfilled these ten ROs. The total delivered ROs are nine. One RO are not delivered because the chips in the bins are not enough. Therefore, LED-CM plant must put forward one MO according to the left one RO to meet the requirements of VMI customers. Besides, the throughput of delivery is 4400k chips and the final left chips are 1489k.

If using the optimal allocation replenishment method, and assume that the potential specification of RO based on the forecast of sale department is the 7th RO. Because the total initial chips in these bins are greater than the total required quantity of the ten ROs, the throughput of delivery must be the total required quantity of the ten ROs. And the delivered ROs must be ten ROs. The first two objectives are modeled as constraints and the third objective, i.e., Equation (9), is the primary objective. The member of the set of hot specifications is the 7th RO, i.e., H= {7}. Therefore, the proposed MACBRO then becomes an integer linear programming model.

| Bi | in # (<i>m</i>) | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | TT |
|------------------|--------------------------------|-----|-----|-----|-----|------------|------------|-----|-----|-----|------|
| Init | . Inv.(<i>b_m</i>) | 455 | 900 | 657 | 757 | 847 | 757 | 551 | 565 | 400 | 5889 |
| RO# (<i>i</i>) | Qty(r _i) | | | | A | llocated Q | uantity (d | im) | | | |
| 1 | 370 | 107 | 265 | | 4 | 4 | | | | | 370 |
| 2 | 440 | 181 | 26 | 233 | | | | | | | 440 |
| 3 | 180 | 167 | | | 6 | | | 7 | | | 180 |
| 4 | 310 | | | 291 | | | 10 | | | 9 | 310 |
| 5 | 430 | | 285 | 133 | | 5 | 7 | | | | 430 |
| 6 | 350 | | 334 | | | 7 | | | 9 | | 350 |
| 7 | 950 | | | | | | | 287 | 466 | 197 | 950 |
| 8 | 1320 | | | | | 423 | 736 | | 23 | 138 | 1320 |
| 9 | 370 | | | | 362 | 4 | 4 | | | | 370 |
| 10 | 1000 | | | | 385 | 404 | | 201 | 10 | | 1000 |
| Final | Inv. (\mathcal{B}_m) | 0 | 0 | 0 | 0 | 0 | 0 | 56 | 57 | 56 | 169 |

Table 6: The Result of Optimal MACBRO for the Example in Table 3 (Unit: k chips)

The problem was solved by LINGO and the result of optimal MACBRO is shown in Table 6. Ten ROs are delivered and the throughput of delivery is 5720k. The final left chips are 169k. Because the feasible bins of the future hot specifications (i.e., 7^{th} RO) are the 7^{th} , 8^{th} , and 9^{th} bin, the left chips are all in these feasible bins as the requirement of the third objective. That is 56k chips in the 7^{th} bin, 57k chips in the 8^{th} bin and 56k chips in the 9^{th} bin respectively. This result will therefore speed up the possibility of being utilized for these left chips in the near future. A comparison of results of two replenishment methods for the example of Table 3 is shown as Table 7.

6.2. Application Case

A model of allocatiing chips from bins to ROs is proposed for the LED-CM plants. An application case of VMI is described as follows.

Assume that the LED-CM plant provides VMI service to three customers, which are X, Y and Z respectively. Integrating the requirements of three VMI customers, the LED-CM plant has twenty ROs. The required chips of these ROs are shown in the first two columns of Table 8. Total required chips of these ROs are 6380k. The specifications of the LED chips in this case are sorted to 25 bins (i.e., 5x5 bins). The feasible bins of these ROs are shown in shadow grids in Table 8. The initial chips (inventory) in each bin are shown in the first two rows of Table 8. Total chips in these bins are 2919k. In order to avoid the upgrade of specification issue, a 1% minimum ratio of quantity is required for a feasible bin of each RO.

In this case, total chips in the bins (i.e., 2919k) are less than the total required chips of these twenty ROs (i.e., 6380k). The objective of this LED-CM plant is to quickly deliver more ROs to meet the requirements of VMI customers. That is the ROs are required to be delivered as the most and the quickest as possible by the plant manager. When we use the average allocation replenishment method, a result of MACBRO for an application case of a LED-CM plant is achieved as shown in Table 8. The total delivered ROs are nine. Eleven ROs are not delivered because the chips in the bins are not enough. Therefore, LED-CM plant must put forward eleven MOs according to the left eleven ROs to meet the requirements of VMI customers. Besides, the throughput of delivery is 1300k chips and the final left chips are 1619k.

| | | Average allocation | Optimal allocation |
|---------------------|------------------------|----------------------|----------------------|
| | | replenishment method | replenishment method |
| | Total ROs | 10 | 10 |
| Requirements of VMI | fulfilled ROs | 9 | 10 |
| warehouse | Not fulfilled ROs (put | 1 | 0 |
| | forward MOs) | 1 | 0 |
| LCD-CM Plant | Initial inventory | 5889 | 5889 |
| Central warehouse | throughput of delivery | 4400 | 5720 |
| (K chips) | Final inventory | 1489 | 169 |

| Table | 7: | Comparison | of Two | Replenishment | Methods for | the Example |
|-------|----|------------|--------|---------------|-------------|-------------|
| | | • | | • | | • |

If using the optimal allocation replenishment method, we assume the potential specifications of RO based on the forecast of sale department are the 4th and 17th ROs in the future. That is the member of the set of hot specifications is the 4th and 17th ROs, i.e., H= {4, 17}. Therefore the last two objectives are modeled as constraints and the first objective, i.e., Equation (7), is the primary objective.

The result of allocation of chips from bins to ROs is shown in Table 9. The throughput of delivery is 2750k chips and the final left chips are 169k. Besides, the total delivered ROs are thirteen. There are seven ROs are failed to be fulfilled. Therefore, LED-CM plant must put forward seven MOs according to the left seven ROs to meet the requirements of VMI customers. Because the future hot specifications are the 4^{th} and 17^{th} ROs, the left chips are all in their feasible bins. That is 88k chips in the 6^{th} bin, 10k chips in the 7^{th} bin, 19k chips in the 11^{th} bin, 10k chips in the 21^{st} and 22^{nd} bin, respectively. This result will further improve the possibility of being utilized for these left chips in the near future.

However, the objective of more ROs of delivery can be changed to higher throughput of delivery to obtain better profit. In this requirement, the first and third objectives are modeled as constraints. And the second objective, i.e., Eq. (8), is the primary objective. After the computation, the throughput of delivery increases to be 2910k chips and the final left chips decrease to be only 9k as shown in Table 10. The total delivered ROs are nine. There are eleven ROs are failed to be fulfilled. Therefore, LED-CM plant must put forward eleven MOs according to the left eleven ROs to meet the requirements of VMI customers.

| Bi | n # | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | TT |
|------|-----------|-----|----|-----|-----|-----|-----|----|----|----|----|----|-------|-------|-------|--------|-------------------|----|-----|-----|-----|-----|----|----|-----|----|------|
| Init | . Inv. | 158 | 93 | 163 | 110 | 100 | 363 | 85 | 75 | 63 | 70 | 75 | 90 | 165 | 85 | 78 | 146 | 35 | 175 | 234 | 115 | 163 | 83 | 30 | 100 | 65 | 2919 |
| RO# | Qty | | | | | | | | | | | A | lloca | ted C | luant | ity (a | 1 _{im}) | | | | | | | | | | |
| 1 | 440 | | | | | | | | | | | | | 73 | 73 | 73 | | | 73 | 74 | 74 | | | | | | 440 |
| 2 | 40 | | | 6 | 6 | | | | 7 | 7 | | | | 7 | 7 | | | | | | | | | | | | 40 |
| 3 | 630 | | | | | | | | | | | | | 0 | 0 | | | | 0 | 0 | | | | 0 | 0 | | 0 |
| 4 | 60 | | | | | | | | | | | 10 | 10 | | | | 10 | 10 | | | | 10 | 10 | | | | 60 |
| 5 | 50 | 8 | 8 | | | | 8 | 8 | | | | 9 | 9 | | | | | | | | | | | | | | 50 |
| 6 | 570 | | | | | | | | | | | | | | | | 0 | 0 | 0 | | | 0 | 0 | 0 | | | 0 |
| 7 | 240 | | | | | | | 43 | 43 | | | | 43 | 43 | | | | 25 | 43 | | | | | | | | 240 |
| 8 | 520 | | | | | | | | | | | | | | | | | 0 | 0 | 0 | | | 0 | 0 | 0 | | 0 |
| 9 | 20 | | | | | | | | | | | | | | 3 | 3 | | | | 3 | 3 | | | | 4 | 4 | 20 |
| 10 | 430 | | | | | | | | | | | | 0 | 0 | 0 | | | | 0 | 0 | 0 | | | | | | 0 |
| 11 | 350 | | | | | | | 0 | 0 | 0 | | | 0 | 0 | 0 | | | | | | | | | | | | 0 |
| 12 | 520 | | | | | | | | | | | | | | 0 | 0 | | | | 0 | 0 | | | | 0 | 0 | 0 |
| 13 | 30 | | 5 | 5 | 5 | | | 5 | 5 | 5 | | | | | | - | | | | | | | | - | | | 30 |
| 14 | 150 | | | | | | | | | 36 | 36 | | | | 2 | 2 | | | | 37 | 37 | | | - | | | 150 |
| 15 | 270 | | | 67 | 67 | 67 | | | 20 | 15 | 34 | | | | | | | | | | | | | | | | 270 |
| 16 | 600 | | | | 0 | 0 | | | | 0 | 0 | | | | 0 | 0 | | | | | | | | | | | 0 |
| 17 | 580 | | | | | | 0 | 0 | | | | 0 | 0 | | | - | 0 | 0 | | | | | | | | | 0 |
| 18 | 540 | 0 | 0 | 0 | | | 0 | 0 | 0 | | | | | | | - | | | | | | | | | | | 0 |
| 19 | 100 | | | | | | | | | | | | | 0 | 0 | | | | 0 | 0 | | | | 0 | 0 | | 0 |
| 20 | 240 | | | | | | | | | | | | | | 0 | 0 | | | | 0 | 0 | | | | 0 | 0 | 0 |
| Fi | nal IV | 150 | 80 | 85 | 32 | 33 | 355 | 29 | 0 | 0 | 0 | 56 | 28 | 42 | 0 | 0 | 136 | 0 | 59 | 120 | 1 | 153 | 73 | 30 | 96 | 61 | 1619 |

Table 8: Results of MACBRO for Case of a LED-CM Plant (Unit: k chips)

| Bi | n # | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | TT |
|-----------|----------|-----|----|-----|-----|-----|-----|----|----|----|----|-----|------|------|------|--------|--------------------|----|-----|-----|-----|-----|----|----|-----|----|------|
| Init. | Inv. | 158 | 93 | 163 | 110 | 100 | 363 | 85 | 75 | 63 | 70 | 75 | 90 | 165 | 85 | 78 | 146 | 35 | 175 | 234 | 115 | 163 | 83 | 30 | 100 | 65 | 2919 |
| RO# | Qty | | | | | | | | | | | All | ocat | ed C | luan | tity (| (d _{im}) | | | | | | | | | | |
| 1 | 440 | | | | | | | | | | | | | 137 | 55 | 6 | | | 5 | 153 | 84 | | | | | | 440 |
| 2 | 40 | | | 3 | 33 | | | | 1 | 1 | | | | 1 | 1 | | | | | | | | | | | | 40 |
| 3 | 630 | | | | | | | | | | | | | 0 | 0 | | | | 0 | 0 | | | | 0 | 0 | | 0 |
| 4 | 60 | | | | | | | | | | | 55 | 1 | | | | 1 | 1 | | | | 1 | 1 | | | | 60 |
| 5 | 50 | 17 | 1 | | | | 29 | 1 | | | | 1 | 1 | | | | | | | | | | | | | | 50 |
| 6 | 570 | | | | | | | | | | | | | | | | 135 | 21 | 165 | | | 151 | 71 | 27 | | | 570 |
| 7 | 240 | | | | | | | 67 | 64 | | | | 78 | 25 | | | | 3 | 3 | | | | | | | | 240 |
| 8 | 520 | | | | | | | | | | | | | | | | | 0 | 0 | 0 | | | 0 | 0 | 0 | | 0 |
| 9 | 20 | | | | | | | | | | | | | | 6 | 2 | | | | 2 | 7 | | | | 1 | 2 | 20 |
| 10 | 430 | | | | | | | | | | | | 0 | 0 | 0 | | | | 0 | 0 | 0 | | | | | | 0 |
| 11 | 350 | | | | | | | 0 | 0 | 0 | | | 0 | 0 | 0 | | | | | | | | | | | | 0 |
| 12 | 520 | | | | | | | | | | | | | | 0 | 0 | | | | 0 | 0 | | | | 0 | 0 | 0 |
| 13 | 30 | | 15 | 10 | 2 | | | 1 | 1 | 1 | | | | | | | | | | | | | | | | | 30 |
| 14 | 150 | | | | | | | | | 58 | 67 | | | | 3 | 14 | | | | 2 | 6 | | | | | | 150 |
| 15 | 270 | | | 86 | 75 | 100 | | | 3 | 3 | 3 | | | | | | | | | | | | | | | | 270 |
| 16 | 600 | | | | 0 | 0 | | | | 0 | 0 | | | | 0 | 0 | | | | | | | | | | | 0 |
| 17 | 580 | | | | | | 0 | 0 | | | | 0 | 0 | | | | 0 | 0 | | | | | | | | | 0 |
| 18 | 540 | 141 | 77 | 64 | | | 246 | 6 | 6 | | | | | | | | | | | | | | | | | | 540 |
| 19 | 100 | | | | | | | | | | | | | 2 | 7 | | | | 2 | 11 | | | | 3 | 75 | | 100 |
| 20 | 240 | | | | | | | | | | | | | | 13 | 56 | | | | 66 | 18 | | | | 24 | 63 | 240 |
| Fii In | nal v | 0 | 0 | 0 | 0 | 0 | 88 | 10 | 0 | 0 | 0 | 19 | 10 | 0 | 0 | 0 | 10 | 10 | 0 | 0 | 0 | 11 | 11 | 0 | 0 | 0 | 169 |

Table 9: Results of Optimal MACBRO for Case of a LED-CM Plant (Unit: k chips) (primary objective: maximizing ROs of delivery)

7. DISCUSSIONS

This sudy uses two different replenishment methods to implement VMI in LED-CM plant. A comparison of result of two replenishment methods for the case of a LED-CM plant is shown as Table 11.

Table 10: ResultS of Optimal MACBRO for Case of a LED-CM Plant (Unit: k chips)

(primary objective: maximizing throughput of delivery)

| Bi | n # | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | TT |
|-------|------|-----|----|-----|-----|-----|-----|----|----|----|----|-----|------|------|------|--------|--------------------|----|-----|-----|-----|-----|----|----|-----|----|------|
| Init. | Inv. | 158 | 93 | 163 | 110 | 100 | 363 | 85 | 75 | 63 | 70 | 75 | 90 | 165 | 85 | 78 | 146 | 35 | 175 | 234 | 115 | 163 | 83 | 30 | 100 | 65 | 2919 |
| RO# | Qty | | | | | | | | | | | All | ocat | ed Q | luan | tity (| (d _{im}) | | | | | | | | | | |
| 1 | 440 | | | | | | | | | | | | | 0 | 0 | 0 | | | 0 | 0 | 0 | | | | | | 0 |
| 2 | 40 | | | 0 | 0 | | | | 0 | 0 | | | | 0 | 0 | | | | | | | | | | | | 0 |
| 3 | 630 | | | | | | | | | | | | | 0 | 0 | | | | 0 | 0 | | | | 0 | 0 | | 0 |
| 4 | 60 | | | | | | | | | | | 0 | 0 | | | | 0 | 0 | | | | 0 | 0 | | | | 0 |
| 5 | 50 | 0 | 0 | | | | 0 | 0 | | | | 0 | 0 | | | | | | | | | | | | | | 0 |
| 6 | 570 | | | | | | | | | | | | | | | | 104 | 24 | 169 | | | 162 | 82 | 29 | | | 570 |
| 7 | 240 | | | | | | | 0 | 0 | | | | 0 | 0 | | | | 0 | 0 | | | | | | | | 0 |
| 8 | 520 | | | | | | | | | | | | | | | | | 0 | 0 | 0 | | | 0 | 0 | 0 | | 0 |
| 9 | 20 | | | | | | | | | | | | | | 0 | 0 | | | | 0 | 0 | | | | 0 | 0 | 0 |
| 10 | 430 | | | | | | | | | | | | 5 | 122 | 62 | | | | 5 | 191 | 45 | | | | | | 430 |
| 11 | 350 | | | | | | | 0 | 0 | 0 | | | 0 | 0 | 0 | | | | | | | | | | | | 0 |
| 12 | 520 | | | | | | | | | | | | | | 0 | 0 | | | | 0 | 0 | | | | 0 | 0 | 0 |
| 13 | 30 | | 1 | 1 | 5 | | | 1 | 3 | 19 | | | | | | | | | | | | | | | | | 30 |
| 14 | 150 | | | | | | | | | 13 | 53 | | | | 5 | 9 | | | | 31 | 39 | | | | | | 150 |
| 15 | 270 | | | 4 | 105 | 100 | | | 13 | 31 | 17 | | | | | | | | | | | | | | | | 270 |
| 16 | 600 | | | | 0 | 0 | | | | 0 | 0 | | | | 0 | 0 | | | | | | | | | | | 0 |

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| 17 | 580 | | | | | | 305 | 67 | | | | 74 | 84 | | | | 40 | 10 | | | | | | | | | 580 |
|----------|----------|-----|----|-----|---|---|-----|----|----|---|---|----|----|----|----|----|----|----|---|----|----|---|---|---|----|----|-----|
| 18 | 540 | 158 | 92 | 158 | | | 57 | 16 | 59 | | | | | | | | | | | | | | | | | | 540 |
| 19 | 100 | | | | | | | | | | | | | 43 | 11 | | | | 1 | 1 | | | | 1 | 43 | | 100 |
| 20 | 240 | | | | | | | | | | | | | | 7 | 69 | | | | 11 | 31 | | | | 57 | 65 | 240 |
| Fi In | nal v | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 2 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 9 |

The average allocation replenishment method is implemented in accordance with order of each RO. The optimal replenishment method is implemented with integrating all of ROs simultaneously. The average allocation replenishment method can achieve the goals of reduce inventory and replenishment requirements. But due to allocation limit, it cannot reach the optimal solution. Less RO can be fulfilled and more MOs will be put forward to meet the requirements of VMI customers. It consumes the least inventory.

For the optimal allocation replenishment method, the results of these two objectives of delivery show that this model can help the planner of LED-CM plant to achieve more ROs of delivery or higher throughput of delivery. If primary objective is maximizing ROs of delivery, then the most ROs can be fulfilled and the least MO will be put forward to meet the requirements of VMI customers. It consumes more inventories.

| | | Average allocation | Optimal allocation met | on replenishment thod |
|---------------------|--------------------------------------|----------------------|---------------------------|--------------------------------|
| | | replenishment method | Max. ROs of delivery | Max. throughput of delivery |
| | Total ROs | 20 | 20 | 20 |
| Requirements of VMI | fulfilled ROs | 9 | 13 | 9 |
| warehouse | Not fulfilled ROs (put forward MOs) | 11 | 7 | 11 |
| LCD-CM Plant | Initial inventory | 2919 | 2919 | 2919 |
| Central warehouse | throughput of delivery | 1300 | 2750 | 2910 |
| (K chips) | Final inventory | 1619 | 169 | 9 |

Table 11: Comparison of Two Replenishment Methods for Case of a LED-CM Plant

If primary objective is maximizing throughput of delivery, then less RO can be fulfilled and more MOs will be put forward to meet the requirements of VMI customers. It consumes the most inventories. If some chips are left over from the chips allocating process, the result will further improve the possibility of being utilized for these left chips in the near future by maximizing the total left chips of the feasible bins of the potential or hot ROs.

Through the optimal replenishment method, it can increase the VMI customer satisfaction by fulfilling more ROs immediately and reduce more inventories and manufacturing overhead.

8. CONCLUSION

Due to customer requirements or to providing better services in order to enhance enterprise competitiveness, the Vendor Managed Inventory (VMI) strategy is applied in LED-CM plant. Implementing VMI in LED-CM plant is a complex task because the special features of specification of a product is usually composed of chips of different bins existed in this plant. Deciding how many chips of each feasible bin must be allocated to a replenishment order (RO) will affect the performance of LED-CM plant to implement VMI.

A model of allocating chips from bins to ROs for LED-CM plants was proposed in this paper. Three objectives, namely, maximizing ROs of delivery, maximizing throughput of delivery and maximizing the total left chips of the feasible bins of potential ROs, are considered in this study to achieve the best performance. A numerical example and an application case of VMI in a real-life LED-CM plant were utilized to demonstrate and evaluate the applicability and effectiveness of the proposed model. The results show that this model can help the planner of LED-CM plants to achieve the most ROs of delivery or the highest throughput of delivery. If some chips are left over from the chips allocating process, the model can further improve the possibility of being utilized for these left chips in the near future. Therefore, the model can help utilize inventory of LED-CM plant and replenish to the VMI customers effectively. Furthermore, the obtained optimal ROs of delivery or throughput of delivery could be a valuable information for LED-CM plants. It is concluded that the proposed method can improve the VMI service in the LED-CM plants.

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